ETM02E-02

EPSON TOYOCOM

Application Manual

Real Time Clock Module

RX-4581NB

Model	Product Number
RX-4581NB	Q41458191000400

EPSON TOYOCOM CORPORATION

NOTICE

- The material is subject to change without notice.
- Any part of this material may not be reproduced or duplicated in any form or any means without the written permission of Epson Toyocom.
- The information, applied circuit, program, usage etc., written in this material is just for reference. Epson Toyocom does not assume any liability for the occurrence of infringing any patent or copyright of a third party. This material does not authorize the licensing for any patent or intellectual copyrights.
- Any product described in this material may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export licence from the Ministry of International Trade and industry or other approval from another government agency.
- You are requested not to use the products (and any technical information furnished, if any) for the development and/or manufacture of weapon of mass destruction or for other military purposes. You are also requested that you would not make the products available to any third party who may use the products for such prohibited purposes.
- These products are intended for general use in electronic equipment. When using them in specific applications that require extremely high reliability such as applications stated below, it is required to obtain the permission from Epson Toyocom in advance.
  / Space equipment (artificial satellites, rockets, etc) / Transportation vehicles and related (automobiles, aircraft, trains, vessels, etc) / Medical instruments to sustain life / Submarine transmitters / Power stations and related / Fire work equipment and security equipment / traffic control equipment / and others requiring equivalent reliability.
- In this manual for Epson Tyocom, product code and marking will still remain as previously identified prior to the merger.Due to the on going strategy of gradual unification of part numbers, please review product code and marking as they will change during the course of the coming months. We apologize for the inconvenience, but we will eventually have a unified part numbering system for Epson Toyocom which will be user friendly.

CONTENTS

Miniature Serial Interface RTC Module

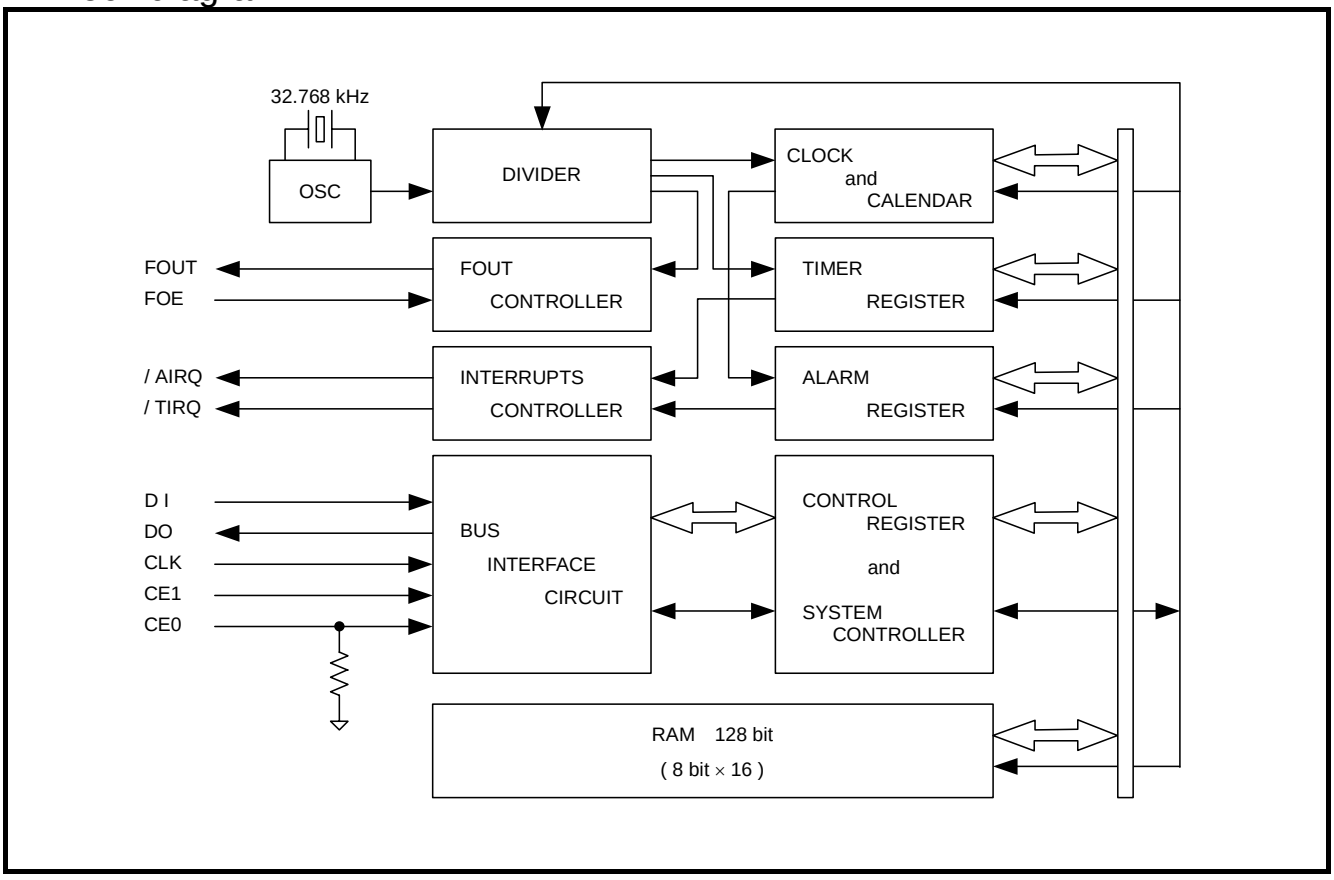
RX – 4581 NB

- Built-in 32.768 kHz crystal oscillator with frequency adjusted
- Serial interface in 4 lines form
  (possible to make it to 3 lines by wired-OR connecting DI and DO pins)
- Alarm interrupt function for day of the week, day, hour, and minute (/AIRQ pin)
- Timer interrupt function (/TIRQ pin)
- Time update interrupt function (second·minute, /AIRQ pin)
- OE function 32.768 kHz output (FOE, FOUT pins)
- Built-in 128 bit (8 bit × 16) RAM
- Automatic adjustment for leap year (supports from year 2000 to 2099)
- Wide range of interface voltage between 1.6 V and 5.5 V
- Wide range of clock (retained) voltage between 1.6 V and 5.5 V
- Low current consumption at 0.4 μA / 3 V (Typ.)
- Available as small package (NB : SON-22 pin PKG.)

1. Overview

This module is a real-time clock with serial interface in 4 lines form (or 3 lines form). It has a built-in crystal oscillator. The module offers many functions such as Clock & Calendar circuitry with automatic leap year adjustment, interval timer, time update interrupt, other rich functions like 32.768 kHz output, and 128 bit (8 bit × 16) RAM. Because it is available in small package SON-22 pin in high density mounting, it is ideally suited for applications such as mobile phone, handy terminals and other small electronic systems.

2. Block diagram

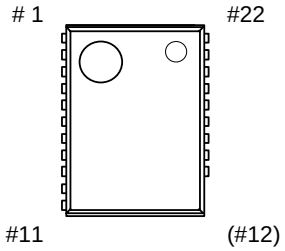


3. Terminal description

3.1. Terminal connections

RX - 4581 NB

1.	GND	22.	N.C.
2.	CE1	21.	N.C.
3.	CE0	20.	N.C.
4.	D I	19.	N.C.
5.	DO	18.	N.C.
6.	CLK	17.	N.C.
7.	/ TIRQ	16.	N.C.
8.	/ AIRQ	15.	N.C.
9.	FOE	14.	N.C.
10.	FOUT	(13)	–
11.	V_{DD}	(12)	–



SON - 22 pin

3.2. Pin functions

Pin name	Pin number	I / O	Functions
GND	1	–	This pin is connected to the minus side (ground) of the power.
CE1	2	Input	This is the chip enabled input pin 1. It does not have a built-in pull-down resistance. When both CE0 and CE1 pins are at the "H" level, access to this RTC becomes possible. Also, when the chip is not selected, the DO pin is at the high impedance level, and the CLK and DI pins would not accept input.
CE0	3	Input	This is the chip enabled input pin 2. It has a built-in pull-down resistance.
D I	4	Input	This is the data input pin for serial data transfer.
DO	5	Output	This is the data output pin for serial data transfer.
CLK	6	Input	This is the shift clock input pin for serial data transfer. In the write mode, it takes in data from the DI pin using the CLK signal rise edge. In the read mode, it outputs data from the DO pin using the fall edge.
/ TIRQ	7	Output	This is the open drain output pin for timer interrupt.
/ AIRQ	8	Output	This is the open drain output pin for alarm and time update interrupts.
FOE	9	Input	This is the input pin for the FOUT output control. When the FOE pin is at the "H" level, the FOUT pin goes into the output state; when it is at the "L" level, the FOUT pin is at the high impedance level.
FOUT	10	Output	This pin outputs the reference clock signal at 32.768 kHz (CMOS output). Depending on the level of the FOE input pin, output from the FOUT pin can be prohibited.
V_{DD}	11	–	This pin is connected to the plus side of the power.
N.C.	14 – 22	–	This pin is not connected to the IC chip. All the N.C. pins are connected collectively with the inside frame. Connect this pin to OPEN, GND, or V_{DD}.

* Be sure to connect a filter capacitor of at least 0.1 μF near V_{DD}–GND.

4. Absolute maximum ratings

GND=0 V

Item	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}	Between V_{DD} and GND	–0.3 to +7.0	V
Input voltage	V_{IN}	Input pin	GND–0.3 to V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	FOUT, DO pins	GND–0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	/AIRQ , /TIRQ pins	GND–0.3 to +8.0	V
Storage temperature	T_{STG}	Stored bare product after unpacking	–55 to +125	°C

5. Recommended operating functions

GND=0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage	V_{DD}	–	1.6	3.0	5.5	V
Clock power voltage	V_{CLK}	–	1.6	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	–40	+25	+85	°C

6. Frequency characteristics

GND=0 V

Item	Symbol	Condition	Rating	Unit
Frequency accuracy	$\Delta f / fo$	Ta= +25 °C, V_{DD}=3.0 V	5 ± 23 (*1)	$\times 10^{-6}$
Frequency voltage characteristics	f / V	Ta= +25 °C, V_{DD}=2.0 V to 5.0 V	± 2 Max.	$\times 10^{-6}$ / V
Frequency temperature characteristics	Top	Ta= –10 °C to +70 °C, V_{DD}= 3.0 V ; reference at +25 °C	+10 / –120	$\times 10^{-6}$
Oscillation start up time	t_{STA}	Ta= +25 °C, V_{DD}=3.0 V	3 Max.	s
Aging	fa	Ta= +25 °C, V_{DD}=3.0 V ; first year	± 5 Max.	$\times 10^{-6}$ / year

*1) Equivalent to 1 minute of monthly deviation (excluding offset).

7. Electrical characteristics

7.1. DC electrical characteristics

*If not specifically indicated, GND=0 V, V_{DD}=1.6 V to 5.5 V, Ta= –40 °C to +85 °C

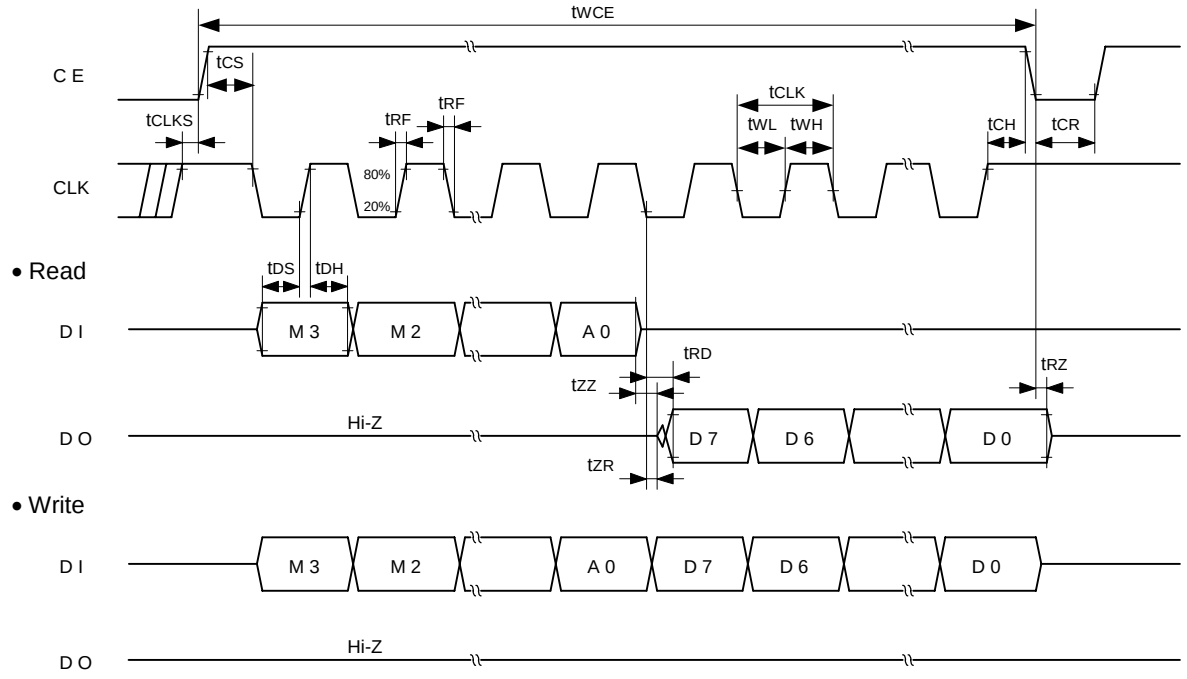
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE0,CE1,FOE = GND /AIRQ, /TIRQ = V_{DD} FOUT ; Output OFF (Hi-z when OFF)	V_{DD}=5 V		0.6	1.2	µA
Current consumption (2)	I_{DD2}		V_{DD}=3 V		0.4	0.8	
Current consumption (3)	I_{DD3}	CE0,CE1 = GND /AIRQ,/TIRQ,FOE = V_{DD} FOUT ; 32.768 kHz output ON, CL=0 pF	V_{DD}=5 V		3.0	7.5	µA
Current consumption (4)	I_{DD4}		V_{DD}=3 V		1.7	4.5	
Current consumption (5)	I_{DD5}	CE0,CE1 = GND /AIRQ,/TIRQ,FOE = V_{DD} FOUT ; 32.768 kHz output ON, CL=30 pF	V_{DD}=5 V		8.0	20.0	µA
Current consumption (6)	I_{DD6}		V_{DD}=3 V		5.0	12.0	
"H" input voltage	V_{IH}	Input pin		0.8 × V_{DD}		V_{DD} + 0.3	V
"L" input voltage	V_{IL}	Input pin		GND – 0.3		0.2 × V_{DD}	V
"H" Output voltage	V_{OH1}	FOUT, DO pins	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
	V_{OH2}		V_{DD}=3 V, I_{OH}=–1 mA	2.0		3.0	
	V_{OH3}		V_{DD}=3 V, I_{OH}=–100 µA	2.9		3.0	
"L" Output voltage	V_{OL1}	FOUT, DO pins	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD}=3 V, I_{OL}=100 µA	GND		GND+0.1	
	V_{OL4}	/AIRQ, /TIRQ pins	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.4	
Input resistance (1)	R_{DWN1}	CE0 pin V_{IN} = V_{DD}	V_{DD}=5 V	75	150	300	kΩ
Input resistance (2)	R_{DWN2}		V_{DD}=3 V	150	300	600	
Input leakage current	I_{LK}	Input pin other than CE0, V_{IN} = V_{DD} or GND		–0.5		0.5	µA
Output leakage current	I_{OZ}	/AIRQ, /TIRQ, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	µA

7.2. AC electrical characteristics

∗If not specifically indicated, GND=0 V, Ta= –40 °C to +85 °C

Item	Symbol	Condition	V_{DD} = 3 V ±10%		V_{DD} = 5 V ±10%		Unit
			Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500		350		ns
CLK H pulse width	t_{WH}		250		175		ns
CLK L pulse width	t_{WL}		250		175		ns
CLK rise and fall time	t_{RF}			100		50	ns
CLK setup time	t_{CLKS}		0		0		ns
CE setup time	t_{CS}		200		150		ns
CE hold time	t_{CH}		200		100		ns
CE recovery time	t_{CR}		300		200		ns
CE enable time	t_{WCE}			0.95		0.95	s
Write data setup time	t_{DS}		100		50		ns
Write data hold time	t_{DH}		100		50		ns
Read data delay time	t_{RD}	C_L=50 pF		200		150	ns
DO output switching time	t_{ZR}			50		20	ns
DO output disable time	t_{RZ}	C_L=50 pF R_L=10 kΩ		200		100	ns
DI/DO conflict avoiding time	t_{ZZ}		0		0		ns
FOUT duty	tw / t	50% V_{DD} level	40	60	40	60	%

Timing chart



∗ If DI and DO pins are wired-OR connected to make it to 3 lines form, secure tzz to avoid bus conflict.

8. How to use

8.1. Registers & RAM

8.1.1. RTC register table (Bank 0)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	SEC	○	40	20	10	8	4	2	1	Permitted	Permitted
1	MIN	○	40	20	10	8	4	2	1	Permitted	Permitted
2	HOUR	○	○	20	10	8	4	2	1	Permitted	Permitted
3	WEEK	○	6	5	4	3	2	1	0	Permitted	Permitted
4	DAY	○	○	20	10	8	4	2	1	Permitted	Permitted
5	MONTH	○	○	○	10	8	4	2	1	Permitted	Permitted
6	YEAR	80	40	20	10	8	4	2	1	Permitted	Permitted
7	RAM	•	•	•	•	•	•	•	•	Permitted	Permitted
8	MIN Alarm	AE	40	20	10	8	4	2	1	Permitted	Permitted
9	HOUR Alarm	AE	•	20	10	8	4	2	1	Permitted	Permitted
A	WEEK Alarm	AE	6	5	4	3	2	1	0	Permitted	Permitted
	DAY Alarm		•	20	10	8	4	2	1		
B	Timer Counter 0	128	64	32	16	8	4	2	1	Permitted	Permitted
C	Timer Counter 1	•	•	•	•	2048	1024	512	256	Permitted	Permitted
D	Extension Register	TEST	WADA	USEL	TE	○	○	TSEL1	TSEL0	Permitted	Permitted *2
E	Flag Register	○	○	UF	TF	AF	○	VLF	○	Permitted	Permitted *6
F	Control Register	○	○	UIE	TIE	AIE	○	STOP	RESET	Permitted	Permitted

∗1. At the initial power supply, the values of the registers are not fixed, so please initialize them before use. While initializing, do not set impossible data for date and time; otherwise there is no guarantee that the clock will operate properly.
∗2. The TEST bit is used by EPSON for testing. Be sure to set it to "0" before use.
∗3. For bits indicated with "○" means write cannot be performed but gets the value 0 when reading. "•" is RAM bit that permits R/W.
∗4. When alarm is not used, addresses between 8 and A can be used as RAM (AIE : "0").
∗5. When the timer counter (addresses B and C) is read, the data value preset previously can be read. When the timer is not used, addresses B and C can be used as RAM (TE,TIE : "0").
∗6. UF, TF, AF, VLF bits are writable only when they are set to "0".

8.1.2. RAM table (Bank 1)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	RAM 0	•	•	•	•	•	•	•	•	Permitted	Permitted
1	RAM 1	•	•	•	•	•	•	•	•	Permitted	Permitted
2	RAM 2	•	•	•	•	•	•	•	•	Permitted	Permitted
⋮	⋮				⋮					⋮	⋮
D	RAM D	•	•	•	•	•	•	•	•	Permitted	Permitted
E	RAM E	•	•	•	•	•	•	•	•	Permitted	Permitted
F	RAM F	•	•	•	•	•	•	•	•	Permitted	Permitted

8.1.3. Selecting R/W for Bank 0 and Bank 1 (outline)

The first 4 bits that sets mode code in the serial communication specify R/W for Bank 0 and Bank 1.
(For details, see the [8.3. Read/Write of data] section.)

Mode	Bank 0 (RTC)	Bank 1 (RAM)
Read	8 h	9 h
Write	0 h	1 h

8.2. Register description

8.2.1. Clock and calendar registers (Reg-0 to Reg-6)

- Data format

  Data is in the BCD format. For example, if the SEC register is set to "0101 1001", this means 59 seconds. The time measurement is in 24-hour format (fixed).

- YEAR register and leap year

  The YEAR register becomes year 00 after year 99.

  Divide the YEAR register's 2-digit BCD by four, and if the remainder is 0, then this year is determined as the leap year. (Year 00 is processed as a leap year. This calendar expires in year 2099.)

- Day of the WEEK register

  The day of the WEEK register is made of 7 bits from 0 to 6. The bits are assigned as shown in the following table.

  Be sure not to set multiple days of week to "1".

bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of the week
0	0	0	0	0	0	**1**	Sunday
0	0	0	0	0	**1**	0	Monday
0	0	0	0	**1**	0	0	Tuesday
0	0	0	**1**	0	0	0	Wednesday
0	0	**1**	0	0	0	0	Thursday
0	**1**	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

8.2.2. Alarm registers (Reg-8 to Reg-A)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN alarm	AE	40	20	10	8	4	2	1
9	HOUR alarm	AE	•	20	10	8	4	2	1
A	WEEK alarm	AE	6	5	4	3	2	1	0
	DAY alarm		•	20	10	8	4	2	1

You can set the day of the week, day, hour and minute for alarm. The WADA bit specifies which alarm is used between the WEEK alarm and the DAY alarm.

Bit 7 is the AE (Alarm Enable) bit for all the alarm registers. By using this bit, you can easily set the hourly alarm and the daily alarm. The day of the week alarm can be set to any multiple days of week.

When the AE bit is set to "0", the appropriate register and the clock register are compared; when the AE bit is set to "1" ("don't care"), the two registers are not compared because they are considered to have the same value.

When the alarm goes off, the AF (Alarm Flag) bit of Reg-E is set to "1"; if at this moment the AIE (Alarm Interrupt Enable) bit of Reg-F has been set to "1", the /AIRQ pin is set to the low level and the interrupt signal occurs. If the AIE bit has been set to "0", the alarm interrupt output from the /AIRQ pin is prohibited.

If alarm interrupt is not used, then addresses 8 to A can be used as memory registers. In this case, set the AIE bit to "0" to prohibit usage of the alarm and alarm interrupt.

- The relationship between the day of the week alarm bit and each day of the week

bit	bit 6	bit 5	Bit 4	bit 3	bit 2	bit 1	bit 0
Day of the week	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

8.2.3. Timer counter (Reg-B and Reg-C)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer counter 0	128	64	32	16	8	4	2	1
C	Timer counter 1	•	•	•	•	2048	1024	512	256

This register controls 12 bits of internal preset-able down counter used for timer interrupt.
TSEL0 and TSEL1 of Reg-D specify the count cycle of the down counter (source clock). Timer counter 0 and timer counter 1 specify the preset value (split cycle) of the down counter.

When the TE bit of Reg-D is set to "0", the preset-able counter loads the content of the timer counter and then stops the counting.
Afterwards, when the TE bit becomes "1", counting starts.

During a source clock cycle, the down counter continues the countdown. When the data becomes zero, the TF (Timer Flag) of Reg-E is set to "1". At this moment, if the TIE (Timer Interrupt Enable) of Reg-F is set to "1", the /TIRQ pin is set to the low level and interrupt signal is generated.
When the TIE bit is set to "0", output from the /TIRQ pin is prohibited.

Next, it reloads the data of timer counter register and restarts the countdown (repeat operation).
Now, when the TE bit is set to "1", even if the timer counter is set with the 0 data, timer interrupt from the /TIRQ pin is not generated. In order to operate timer expectedly, you need to set the TE bit and the TIE bit.

If timer interrupt is not used, then addresses B and C may be used as memory registers. In this case, set TE bit and TIE bit to "0", and prohibit timer operation and timer interrupts.

• Timer interrupt and source clock selection

TSEL1	TSEL0	Source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	Update in minutes

• Timer interrupt interval

Timer counter setting value	Source clock			
	4096 Hz	64 Hz	1 Hz	Update in minutes
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

8.2.4. Control register and flag register (between Reg-D and Reg-F)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension register	TEST	WADA	USEL	TE	○	○	TSEL1	TSEL0
E	Flag register	○	○	UF	TF	AF	○	VLF	○
F	Control register	○	○	UIE	TIE	AIE	○	STOP	RESET

- TEST bit: this bit is used by EPSON for testing.
  Be sure to set this bit to "0". Be careful not to set this bit to "1" when writing to other bits of Reg-D.
  It can be cleared by setting the CE0 pin or the CE1 pin to "L".

- WADA bit (WEEK Alarm / DAY Alarm)
  This bit sets either the WEEK alarm or the DAY alarm. If this bit is set to "0", the information in Reg-A is considered to be for the WEEK alarm. If this bit is set to "1", the information in Reg-A is considered to be for the DAY alarm.

- USEL bit (Update Interrupt Select)
  Specify the occurrence timing of time update interrupt.
  [Selection of timing for time update interrupt]

USEL	Timing	Auto recovery time
0	Update in seconds	7.813 ms
1	Update in minutes	7.813 ms

- TE bit (Timer Enable)
  The moment this bit is set to "1", the preset-able counter begins to count down. When this bit is set to "0", the preset-able counter stops to count down.

- AF bit, TF bit, and UF bit (Alarm Flag, Timer Flag, Update Flag)
  When the alarm goes off, the AF bit is set to "1". When the down counter for timer interrupt is 0, the TF bit is set to "1". At the end of time update, the UF bit is set.
  For these bits, data is retained until writing over them with "0". You cannot write "1" over these bits.

- AIE bit, TIE bit, and UIE bit (Alarm, Timer, Update Interrupt Enable)
  These bits determine whether or not to generate signals when alarm, timer, or time update interrupt event occur.
  AIE corresponds to alarm interrupt, TIE corresponds to timer interrupt, and UIE corresponds to time update interrupt.

- VLF (Voltage Low Flag)
  This flag is used for detecting oscillation stop caused by power voltage drop. When oscillation stop is detected, this bit is set to "1". This information is retained until writing over it with "0".
  This bit is not influenced by states of the other bits such as the STOP bit and the RESET bit.

- STOP bit
  When this bit is set to "1", the operation of counting up the seconds in the Clock & Calendar circuitry is stopped, which stops the clock. When this bit is set to "0", the clock resumes its operation.

- RESET bit
  When this bit is set to "1", values (less than seconds) of the counter in the Clock & Calendar circuitry is reset, and the clock also stops.
  After "1" is written to this bit, this can be released by setting CE to "L".

8.3. Read/Write of data

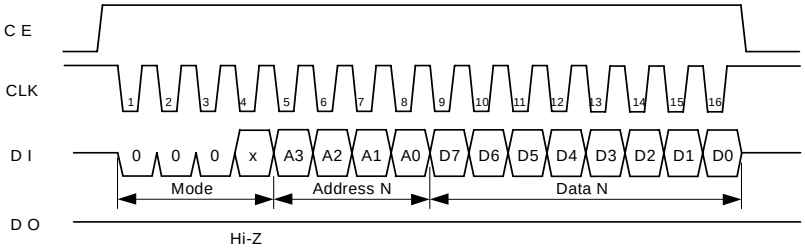
For both read and write, first set up chip condition (internally CE="H") to CE0="H" and CE1="H", then specify the 4-bits address, and finally read or write in 8-bits units.

Both read and write use MSB-first. In continuous operation, objected address is auto incremented.

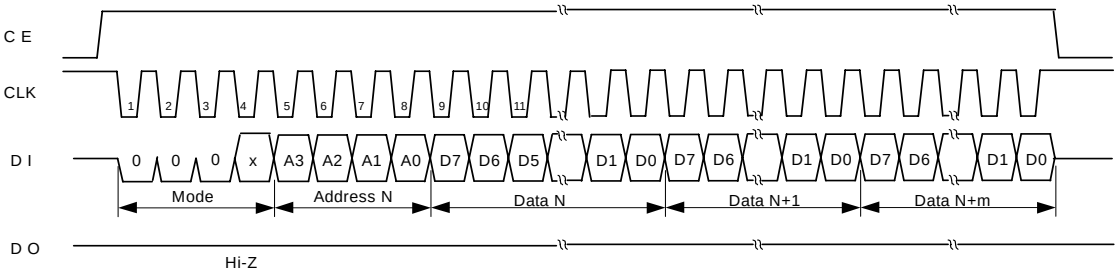
Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

8.3.1. Write of data

1) One-shot writing



2) Continuous writing

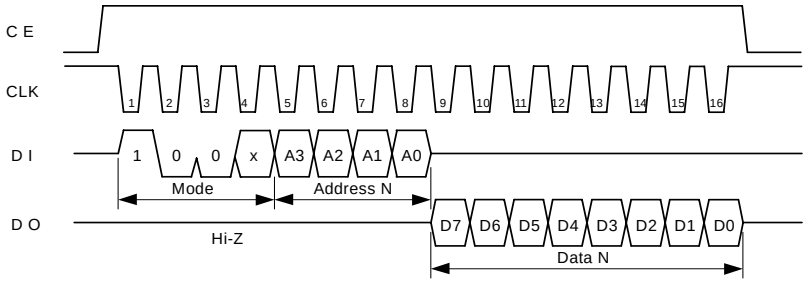


*When writing data, the data needs to be entered in 8-bits units.

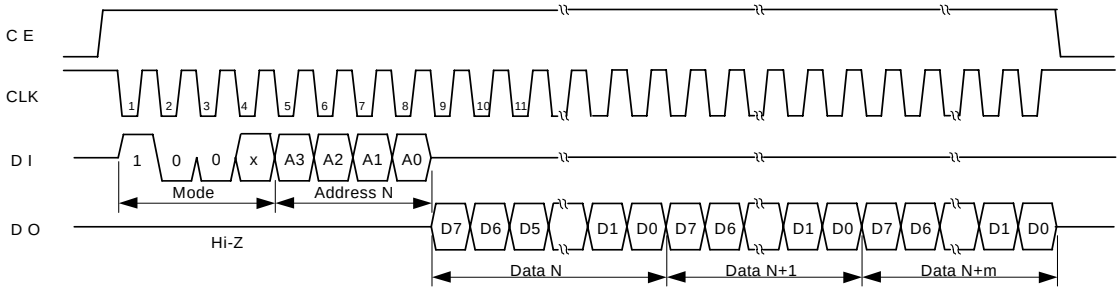
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

8.3.2. Read of data

1) One-shot reading



2) Continuous reading



8.3.3. Write/Read mode setting code for each bank

Mode	Bank 0 (RTC)	Bank 1 (RAM)
Read	8 h	9 h
Write	0 h	1 h

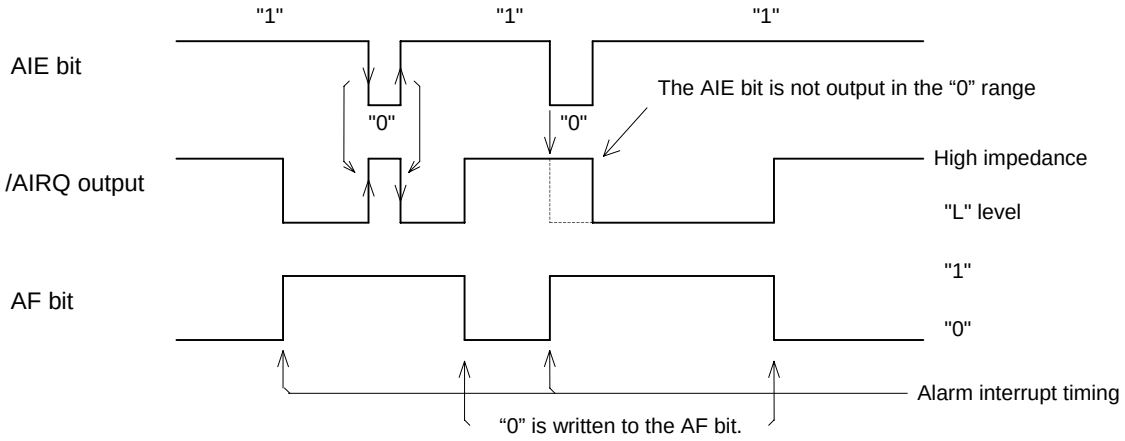
*In the mode setting code, if a value other than those listed is used, the subsequent data will be ignored and the DO pin remains in the Hi-z state.

8.4. Alarm interrupt / Timer interrupt

8.4.1. Alarm interrupt

When the alarm matches and AIE=1, the /AIRQ pin outputs "L"; when AIE=0, the /AIRQ pin is at the high impedance level.

Alarm interrupt is output when "carry" from the 10-second digit to minute digit occurs.



- How to use

The day of the week, day, hour and minute can be set. The WADA bit specifies which alarm is used between the WEEK alarm and the DAY alarm. For the day of the week, multiple days can be set at one time.

To avoid unintended hardware interrupt during the alarm setup, it is recommended that AIE bit be initially set to "0".

Then, set up the alarm data, and apply zero clear to the AF flag in order to initialize (with certainty) the alarm circuitry. Afterward, set the AIE bit to "1". If you desire no hardware interrupt, set the AIE bit to "0", and monitor the AF bit with software as required.

- Usage example

1) Set the alarm to go off at 6 pm tomorrow.

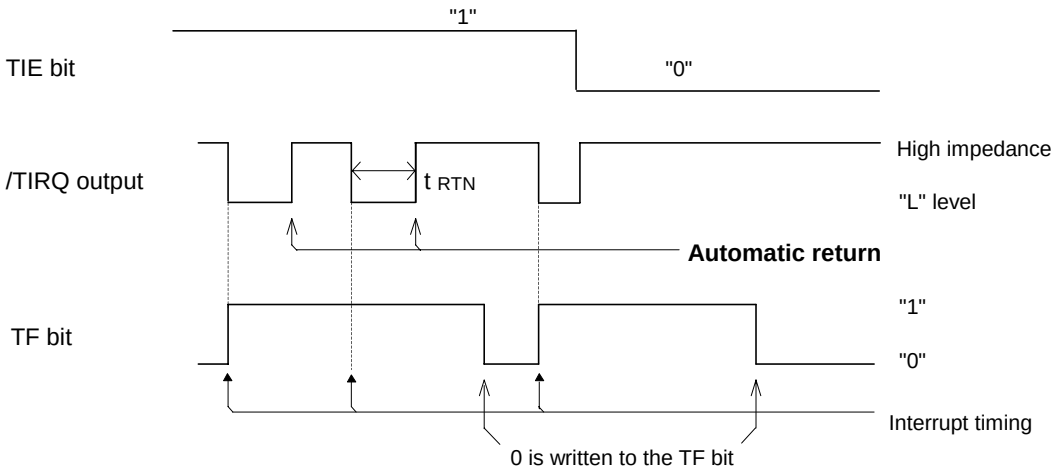
· Write "0" to the AIE bit.
· Write "00h" to the MIN alarm register.
· Write "18h" to the HOUR alarm register.
·· Write tomorrow’s date to the WEEK/DAY alarm register.
· Write "1" to the WADA bit (selecting the DAY alarm).
· Clear the AF bit to zero.
· Write "1" to the AIE bit.

2) Set the alarm to go off at 6 am every morning except Saturdays and Sundays.

· Write "0" to the AIE bit.
· Write "00h" to the MIN alarm register.
· Write "06h" to the HOUR alarm register.
· Write "3Eh" to the WEEK/DAY alarm register.
· Write "0" to the WADA bit (selecting the WEEK alarm).
· Clear the AF bit to zero.
· Write "1" to the AIE bit.

8.4.2. Timer interrupt

· If TIE="1" when interrupt occurs, the /TIRQ pin outputs "L".
· If TIE="0" when interrupt occurs, the /TIRQ pin enters the high impedance state and the TF bit becomes "1", and remains so.



∗ Automatic return

The automatic return time (tRTN) is determined by the source clock specified in Reg-D.

Source clock	Automatic return time (tRTN)
4096 Hz	122 μs
64 Hz	7.813 ms
1 Hz	7.813 ms
Update in minutes	7.813 ms

• Timer measurement error

Because the timer error is $^{+0}/_{-1}$ cycle time of the selected source clock, the set time of the timer falls into the following range:

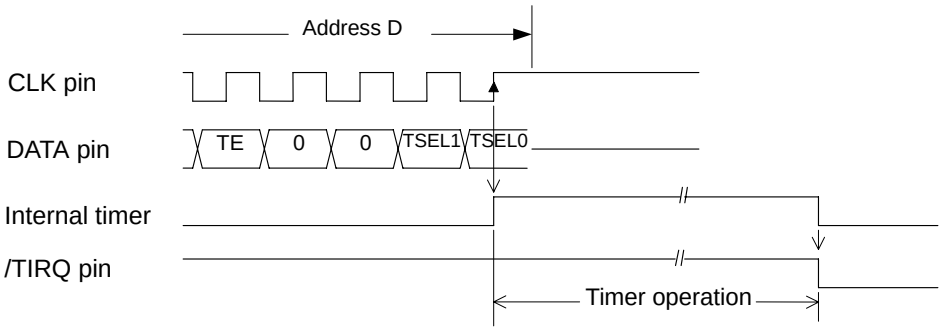
(Set time of the timer (∗) − Source clock cycle) to (Set time of the timer)

∗) Set time of the timer = Source clock cycle × Value of the timer counter.

Now, the actual time of the timer is the above time, plus the communication duration of the serial data transfer clock.

• Timer start timing

In the data write mode, the timer starts counting from the rise edge of the CLK when writing to address D as shown in the following time chart.



• How to use

At the cycle (source clock) specified in the timer interrupt setup register, the countdown starts from the value of the timer counter. When the data becomes zero, the /TIRQ pin becomes "L" and interrupt occurs.

It can be used as an interval timer between a minimum of 1/4096 second to a maximum of 4095 minutes.

To avoid unintended hardware interrupt during the timer setup, setting both TF bit and TIE bit, in the beginning, is recommended.

If you do not want to use any timer interrupt, set TIE bit to "0", and monitor the TF bit with software as required.

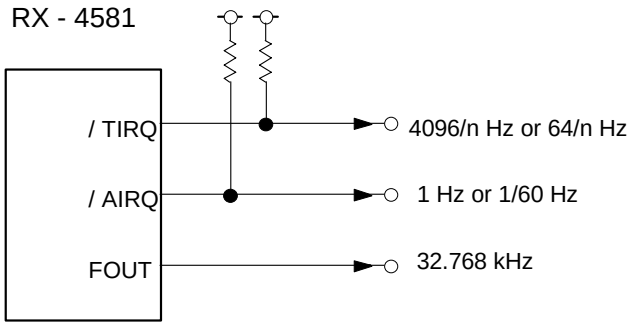
8.5. Reference clock signal output

In RX-4581, each of the /TIRQ pin, the /AIRQ pin and the FOUT pin can output a reference clock at the same time. So three types of reference clock is output at the same time.

By repeating timer interrupt operation from the /TIRQ pin, you can output 4096/n Hz clock signal (when the source clock is 4096 Hz) or 64/n Hz clock signal (when the source clock is 64 Hz).

By causing time update interrupt from the /AIRQ pin, you can output 1 Hz clock signal or 1/60 Hz clock signal.

From the FOUT pin, you can output 32.768 kHz clock signal.



8.6. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup

- Many of this product's operations are linked to the internal quartz oscillator's clock signal, so normal operation is not possible if there is no internal oscillation (= oscillation is stopped).

  Therefore, we recommend that the initial setting to be set during power-on initialization or backup and restore operations (i.e., when the power supply voltage is recovered after oscillation has stopped due to a voltage drop, etc.) should be "first start internal oscillation, then wait for the oscillation stabilization time (see tSTA standard) to elapse".

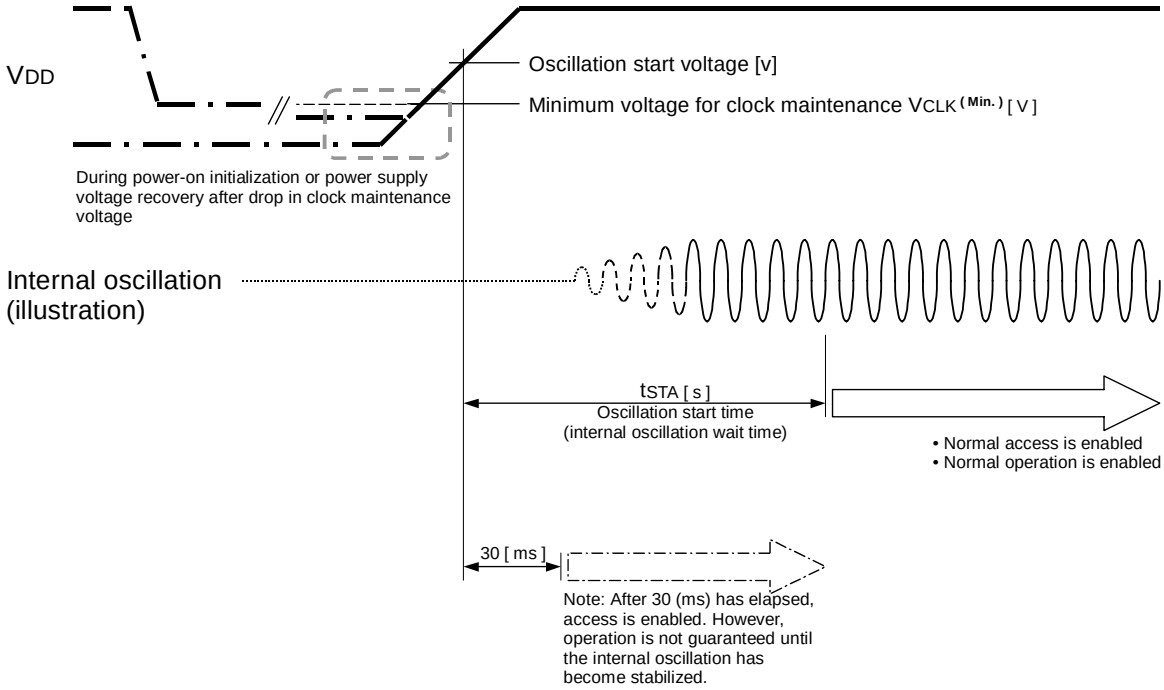
- Note the following caution points concerning access operations during power-on initialization or when restoring the power supply voltage from backup mode (hereafter referred to as "switching to the operating voltage").

  1) Before switching to the operating voltage, read the VLF-bit (which indicates the RTC error status).

  2) Initialization is required when the value read from the VLF-bit is "VLF = 1 (error status)".
  Before initializing in response to this VLF = "1" result, we recommend first waiting for the internal oscillation stabilization time (see the tSTA standard) to elapse.

Initialization is required when the status after reading a VLF-bit value of "1" is either of the following. (Status 1) During power-on initialization (Status 2) When the clock setting is invalid, such as due to a voltage drop during backup

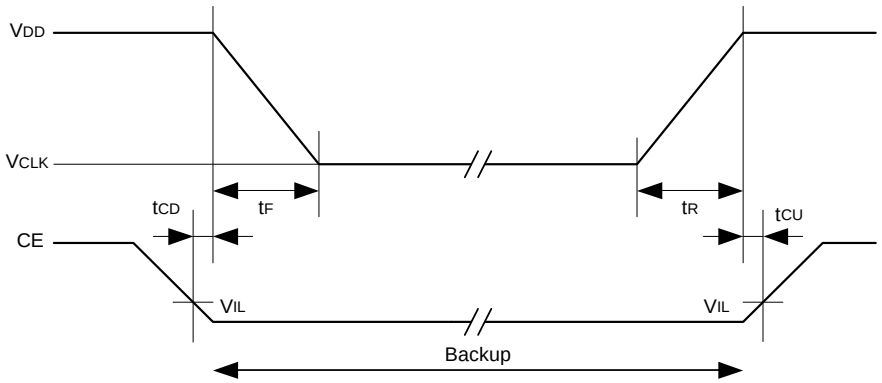
∗ Access timing during power-on initialization and when recovering the power supply voltage after a drop in the voltage used to maintain the clock



  3) When the read VLF-bit value is "VLF = 0 (normal status)", access is enabled without waiting for stabilization of oscillation.

Normal operation is enabled under the following two statuses when "0" is read as the VLF-bit value. (Status 1) When correct operation is enabled (except for settings errors while in use) (Status 2) When data is retained normally while switching to the operating voltage from backup mode

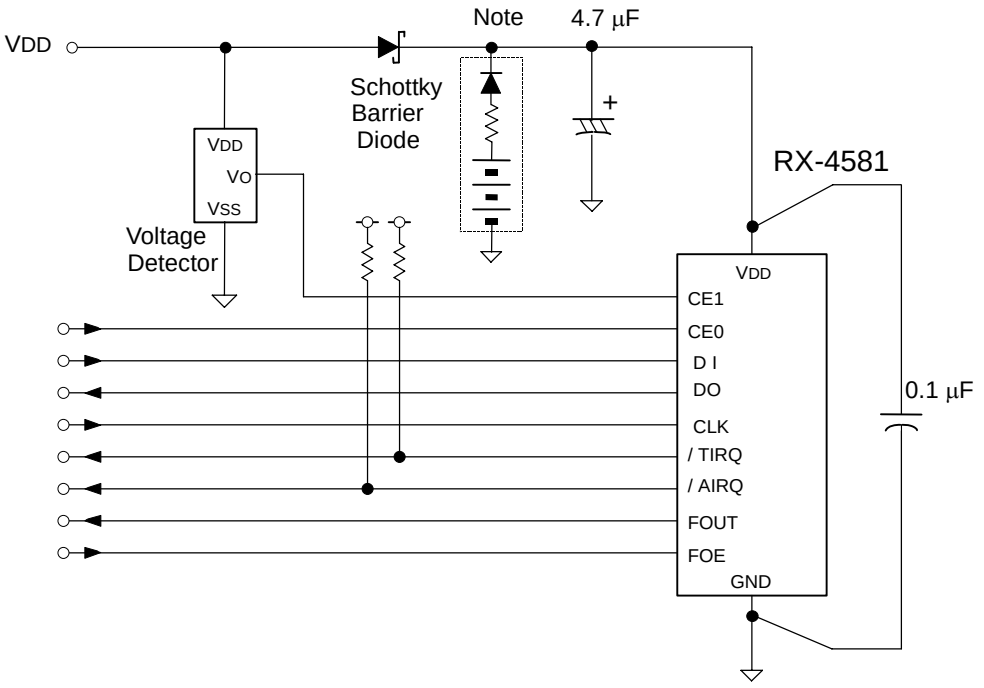
8.7. Shifting to backup and returning



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CE time before power drop	tCD	-	0			μs
Power drop time	tF	-	2			μs/ V
Power rise time	tR	-	1			μs/ V
CE time after power rise	tCU	-	0			μs

* When RTC switch into the backup-mode, CE keeps low level sure and, set the RTC into a disable state.

8.8. External connection example



Note :
Use the secondary battery or a lithium battery. If using the secondary battery, a diode is not necessary. If using a lithium battery, a diode is necessary. For information on resistance value, please consult the battery manufacturer.

9. External dimension / Marking layout

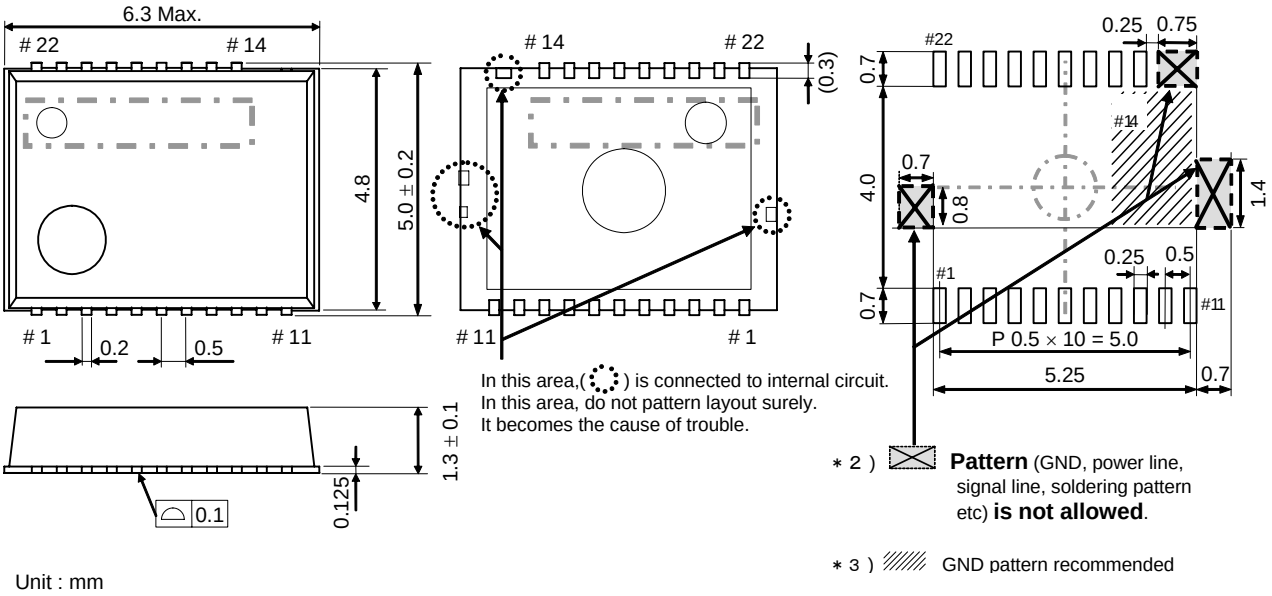
9.1. External dimension

RX – 4581 NB (SON – 22pin)

• External dimensions

• Soldering pattern

∗ In this area(,),pattern layout is not allowed.



Unit : mm

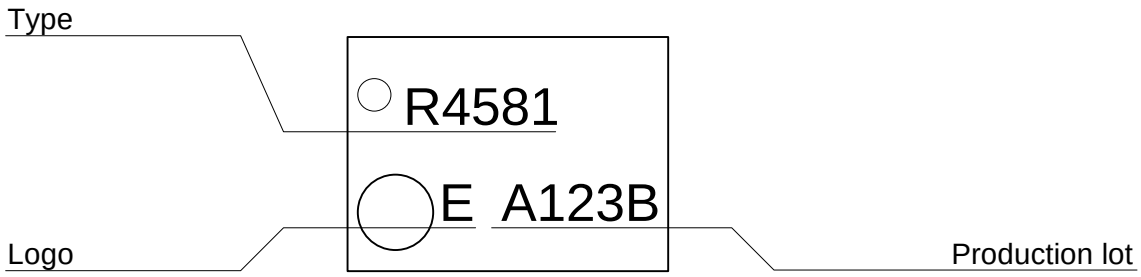
∗ 1) The cylinder of the crystal oscillator may be exposed in this area (top and bottom), however it has no affect on the performance of the device.

∗ 2) Pattern (GND, power line, signal line, soldering pattern, etc) is not allowed.
In this area, at a parts side of board, do not pattern layout surely.
∗ In an area ( ) of the product bottom side, a terminal connected to an IC inside is exposed.
When the circuit pattern contacts those terminal, it will cause serious obstruction to the oscillation, function or electronic spec.

∗ 3) It is the best design that there is no signal line in this area.
Please fill it up with GND pattern if possible.

9.2. Marking layout

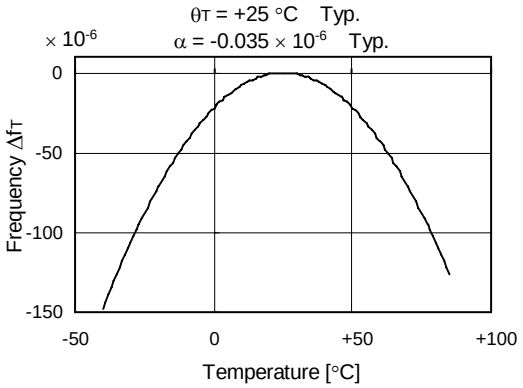
RX – 4581 NB (SON – 22pin)



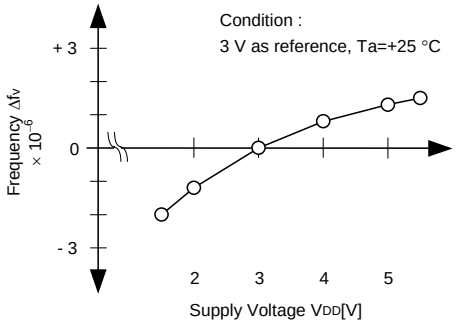
∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

10. Reference data

(1) Example of frequency and temperature characteristics



(2) Example of frequency and voltage characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha\ (\theta_T - \theta_X)^2$

Δf_T		Frequency deviation in any temperature
α	l / °C^2)	Coefficient of secondary temperature (–0.035±0.005) × 10^{-6} / °C^2
θ_T	°C)	Ultimate temperature (+25±5 °C)
θ_X	°C)	Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta F_V$

$\Delta f/f$	Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	Frequency precision
Δf_T	Frequency deviation in any temperature
Δf_V	Frequency deviation in any voltage

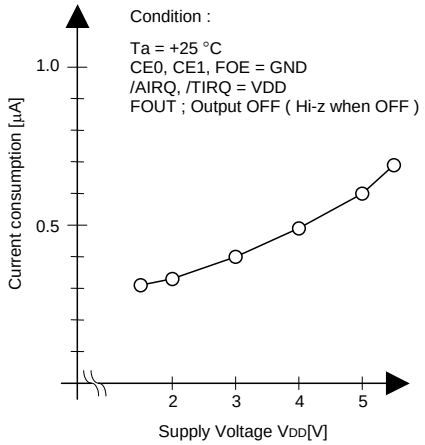
3. How to find the date difference

Date difference = $\Delta f/f \times 86400$ (seconds)

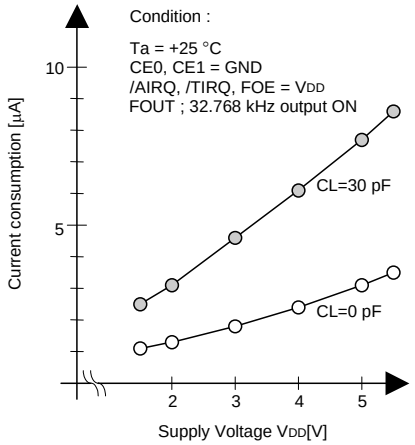
* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(3) Current and voltage consumption characteristics

(3-1) Current consumption when non-accessed (i) when FOUT=OFF



(3-2) Current consumption when non-accessed (ii) when FOUT=32.768 kHz



11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Fig.1 It is the best design that there is no signal line in this area. Please fill it up with GND pattern if possible.
* Fig.1 Pattern (GND, power line, signal line, soldering pattern, etc) is not allowed. In this area, at a parts side of board, do not pattern layout surely.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Caution of pattern layout.

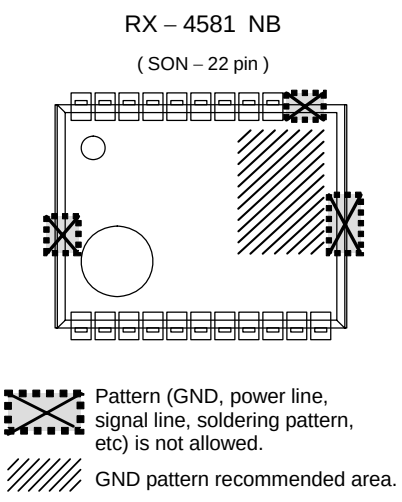
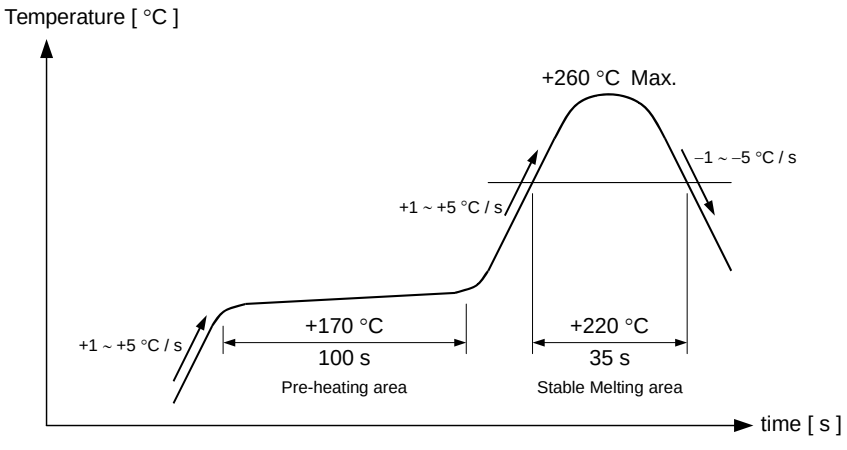


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



EPSON TOYOCOM

Application Manual

AMERICA

EPSON ELECTRONICS AMERICA, INC.

HEADQUARTER	150 River Oaks Parkway, San Jose, CA 95134, U.S.A. Phone: (1)800-228-3964 (Toll free) : (1)408-922-0200 (Main) Fax: (1)408-922-0238 http://www.eea.epson.com
Atlanta Office	One Crown Center 1895 Phoenix Blvd. Suite 348 Atlanta,GA 30349 Phone: (1)800-228-3964 (Toll free) : (1)770-907-7667 (Main)
Boston Office	301Edgewater Place, Ste. 120, Wakefield, MA 01880, U.S.A. Phone: (1)800-922-7667 (Toll free) : (1)781-246-3600 (Main) Fax: (1)781-246-5443
Chicago Office	101 Virginia St., Ste. 290, Crystal Lake, IL 60014, U.S.A. Phone: (1)800-853-3588 (Toll free) : (1)815-455-7630 (Main) Fax: (1)815-455-7633
El Segundo Office	1960 E. Grand Ave., 2nd Floor, El Segundo, CA 90245, U.S.A. Phone: (1)800-249-7730 (Toll free) : (1)310-955-5300 (Main) Fax: (1)310-955-5400

EUROPE

EPSON EUROPE ELECTRONICS GmbH

HEADQUARTER	Riesstrasse 15, 80992 Munich, Germany Phone: (49)-(0)89-14005-0 Fax: (49)-(0)89-14005-110 http://www.epson-electronics.de
Düsseldorf Branch Office	Altstadtstrasse 176, 51379 Leverkusen, Germany Phone: (49)-(0)2171-5045-0 Fax: (49)-(0)2171-5045-10
UK & Ireland Branch Office	Unit 2.4, Doncastle House, Doncastle Road, Bracknell,Berkshire RG12 8PE, England Phone: (44)-(0)1344-381700 Fax: (44)-(0)1344-381701
French Branch Office	LP 915 Les Conquérants, 1 Avenue de l' Atlantique, Z.A. de Courtaboeuf 2 91976 Les Ulis Cedex, France Phone: (33)-(0)1-64862350 Fax: (33)-(0)1-64862355

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSangHuan ChaoYang District, Beijing, China
Phone: (86) 10-6410-6655 Fax: (86) 10-6410-7319
http://www.epson.com.cn

Shinghai Branch: High-Tech Building,900 Yishan Road Shanghai 200233,China
Phone: (86) 21-5423-5577 Fax: (86) 21-5423-4677

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road, Wanchai,Hong kong
Phone: (852) 2585-4600 Fax: (852) 2827-2152
http://www.epson.com.hk

EPSON ELECTRONIC TECHNOLOGY DEVELOPMENT (SHENZHEN)CO., LTD.
12/F, Dawning Mansion,#12 Keji South Road, Hi-Tech Park,Shenzhen, China
Phone: (86) 755-26993828 Fax: (86) 755-26993838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No.7, Song Ren Road, Taipei 110
Phone: (886) 2-8786-6688 Fax: (886)2-8786-6660
http://www.epson.com.tw

EPSON SINGAPORE PTE. LTD.
No 1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633.
Tel: (65)- 6-586-5500 Fax: (65) 6-271-3182
http://www.epson.com.sg

SEIKO EPSON CORPORATION KOREA Office
50F, KLI 63 Building,60 Yoido-dong, Youngdeungpo-Ku, Seoul, 150-763, Korea
Phone: (82) 2-784-6027 Fax: (82) 2-767-3677
http://www.epson-device.co.kr

Gumi Branch Office: 2F, Grand Bldg,457-4, Songjeong-dong Gumi-City,Gyongsangbuk-Do,
730-090, Korea
Phone: (82) 54-454-6027 Fax: (82) 54-454-6093

EPSON TOYOCOM CORPORATION

Distributor

Electronic devices information on WWW server

http://www.epsontoyocom.co.jp